4.1 Introduction
Switch-mode dc-to-ac inverters are used in ac motor drives and uninterruptible ac power supplies where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. As an example, consider an ac motor drive, shown in Fig.4.1 in a block diagram form. The dc voltage is obtained by rectifying and filtering the line voltage, most often by the diode rectifier circuits. In an ac motor load, the voltage at its terminals is desired to be sinusoidal and adjustable in its magnitude and frequency. This is accomplished by means of the switch-mode dc-to-ac inverter of Fig.4.1, which accepts a dc voltage as the input and produces the desired ac voltage input.

To be precise, the switch-mode inverter in Fig.4.1 is a converter through which the power flow is reversible. However, most of the time the power flow is from the dc side to the motor on the ac side, requiring an inverter mode of operation. Therefore, these switch-mode converters are often referred to as switch-mode inverters.

To slow down the ac motor in Fig.4.1, the kinetic energy associated with the inertia of the motor and its load is recovered and the ac motor acts as a generator. During the so-called braking of the motor, the power flows from the ac side to the dc side of the switch-mode converter and it operates in a rectifier mode. The energy recovered during the braking of the ac motor can be dissipated in a resistor, which can be switched in parallel with the dc bus capacitor for this purpose in Fig.4.1. However, in applications where this braking is performed frequently, a better alternative is regenerative braking where the energy recovered from the motor load inertia is fed back to the utility grid, as shown in the system of Fig.4.2. This requires that the converter connecting the drive to the utility grid be a two-quadrant converter with a reversible dc current, which can operate as a rectifier during the motoring mode of the ac motor and as an inverter during the braking of the motor. Such a reversible-current two-quadrant converter can be realized by two back-to-back connected line-frequency thyristor converters or by means of a switch-mode converter as shown in Fig.4.2. There are other reasons for using such a switch-mode rectifier (called a rectifier because, most of the time, the power flows from the ac line input to the dc bus) to interface the drive with the utility system.

![Fig.4.1 Switch mode inverter in ac motor drive.](image1)

![Fig.4.2 Switch-mode converters for motoring and regenerative braking in ac motor drive.](image2)

In this chapter, we will discuss inverters with single-phase and three-phase ac outputs. The input to switch-mode inverters will be assumed to be a dc voltage source, as was assumed in the block
diagrams of Fig.4.1 and Fig.4.2. Such inverters are referred to as voltage source inverters (VSIs). The other types of inverters, now used only for very high power ac motor drives, are the current source inverters (CSIs), where the dc input to the inverter is a dc current source. Because of their limited applications, the CSIs are not discussed.

The VSIs can be further divided into the following three general categories:

1. Pulse-width-modulated inverters. In these inverters, the input dc voltage is essentially constant in magnitude, such as in the circuit of Fig.4.1, where a diode rectifier is used to rectify the line voltage. Therefore, the inverter must control the magnitude and the frequency of the ac output voltages. This is achieved by PWM of the inverter switches and hence such inverters are called PWM inverters. There are various schemes to pulse-width modulate the inverter switches in order to shape the output ac voltages to be as close to a sine wave as possible. Out of these various PWM schemes, a scheme called the sinusoidal PWM will be discussed in detail, and some of the other PWM techniques will be described in a separate section at the end of this chapter.

2. Square-wave inverters. In these inverters, the input dc voltage is controlled in order to control the magnitude of the output ac voltage, and therefore the inverter has to control only the frequency of the output voltage. The output ac voltage has a waveform similar to a square wave, and hence these inverters are called square-wave inverters.

3. Single-phase inverters with voltage cancellation. In case of inverters with single-phase output, it is possible to control the magnitude and the frequency of the inverter output voltage, even though the input to the inverter is a constant dc voltage and the inverter switches are not pulse-width modulated (and hence the output voltage wave-shape is like a square wave). Therefore, these inverters combine the characteristics of the previous two inverters. It should be noted that the voltage cancellation technique works only with single-phase inverters and not with three-phase inverters.

4.2 BASIC CONCEPTS OF SWITCH-MODE INVERTERS

In this section, we will consider the requirements on the switch-mode inverters. For simplicity, let us consider a single-phase inverter, which is shown in block diagram form in Fig.4.3a, where the output voltage of the inverter is filtered so that \( v_o \) can be assumed to be sinusoidal. Since the inverter supplies an inductive load such as an ac motor, \( i_o \) will lag \( v_o \), as shown in Fig.4.3b. The output waveforms of Fig.4.3b show that during interval 1, \( v_o \) and \( i_o \) are both positive, whereas during interval 3, \( v_o \) and \( i_o \) are both negative. Therefore, during intervals 1 and 3, the instantaneous power flow \( p_o = v_o \times i_o \) is from the dc side to the ac side, corresponding to an inverter mode of operation. In contrast, \( v_o \) and \( i_o \) are of opposite signs during intervals 2 and 4, and therefore \( p_o \) flows from the ac side to the dc side of the inverter, corresponding to a rectifier mode of operation. Therefore, the switch-mode inverter of Fig.4.3a must be capable of operating in all four quadrants of the \( i_o - v_o \) plane, as shown in Fig.4.3c during each cycle of the ac output. Such a four-quadrant inverter is reversible and \( v_o \) can be of either polarity independent of the direction of \( i_o \). Therefore, the full-bridge converter meets the switch-mode inverter requirements. Only one of the two legs of the full-bridge converter, for example leg A, is shown in Fig.4.4. All the dc-to-ac inverter topologies described in this chapter are derived from the one-leg converter of Fig.4.4. For ease of explanation, it will be assumed that in the inverter of Fig.4.4, the midpoint "o" of the dc input voltage is available, although in most inverters it is not needed and also not available.
To understand the dc-to-ac inverter characteristics of the one-leg inverter of Fig.4.4, we will first assume that the input dc voltage $V_d$ is constant and that the inverter switches are pulse-width modulated to shape and control the output voltage. Later on, it will be shown that the square-wave switching is a special case of the PWM switching scheme.

4.2.1 PULSE-WIDTH-MODULATED SWITCHING SCHEME

In inverter circuits, we would like the inverter output to be sinusoidal with magnitude and frequency controllable. In order to produce a sinusoidal output voltage waveform at a desired frequency, a sinusoidal control signal at the desired frequency is compared with a triangular waveform, as shown in Fig.4.5a. The frequency of the triangular waveform establishes the inverter switching frequency and is generally kept constant along with its amplitude $V_{tri}$.

Before discussing the PWM behavior, it is necessary to define a few terms. The triangular waveform $V_{tri}$ in Fig.4.5a is at a switching frequency $f_s$ which establishes the frequency with which the inverter switches are switched ($f_s$ is also called the carrier frequency). The control signal $v_{control}$ is used to modulate the switch duty ratio and has a frequency $f_1$, which is the desired fundamental frequency of the inverter voltage output ($f_1$ is also called the modulating frequency), recognizing that the inverter output voltage will not be a perfect sine wave and will contain voltage components at harmonic frequencies of $f_1$. The amplitude modulation ratio $m_a$ is defined as
\[ m_a = \frac{\hat{V}_{\text{control}}}{\hat{V}_{\text{tri}}} \]  

(4.1)

where \( \hat{V}_{\text{control}} \) is the peak amplitude of the control signal. The amplitude \( \hat{V}_{\text{tri}} \) of the triangular signal is generally kept constant.

The frequency modulation ratio \( m_f \) is defined as:

\[ m_f = \frac{f_s}{f_1} \]  

(4.2)

In the inverter of Fig.4.4b, the switches \( T_{A+} \) and \( T_{A-} \) are controlled based on the comparison of \( v_{\text{control}} \) and \( v_{\text{tri}} \) and the following output voltage results, independent of the direction of \( i_o \):

\[ v_{\text{control}} > v_{\text{tri}} \quad T_{A+} \text{ is on} , \quad v_{AO} = \frac{1}{2} V_d \]  

(4.3)

\[ v_{\text{control}} < v_{\text{tri}} \quad T_{A-} \text{ is on} , \quad v_{AO} = -\frac{1}{2} V_d \]

Fig.4.5 Pulse width modulation.
Since the two switches are never off simultaneously, the output voltage $V_{ao}$ fluctuates between two values ($\frac{1}{2}V_d$ and $-\frac{1}{2}V_d$). Voltage $v_{ao}$ and its fundamental frequency component (dashed curve) are shown in Fig.4.5b, which are drawn for $m_f = 15$ and $m_a = 0.8$. The harmonic spectrum of $v_{ao}$ under the conditions indicated in Figs.4.5a and Fig.4.5b is shown in Fig.4.5c, where the normalized harmonic voltages $(\hat{V}_{ao})_h/\frac{1}{2}V_d$ having significant amplitudes are plotted. This plot (for $m_a \leq 1.0$) shows three items of importance:

1. The peak amplitude of the fundamental-frequency component $(\hat{V}_{ao})_0$ is $m_a$ times $V_d/2$. This can be explained by first considering a constant $v_{control}$, as shown in Fig.4.6a. This results in an output waveform $\hat{v}_{ao}$. From the PWM in a full-bridge dc-dc converter, it can be noted that the average output voltage (or more specifically, the output voltage averaged over one switching time period $T_s = 1/f_s$) $v_{ao}$ depends on the ratio of $v_{control}$ to $\hat{v}_{tri}$ for a given $V_d$:

$$v_{ao} = \frac{v_{control}}{\hat{v}_{tri}} \frac{V_d}{2} \quad v_{control} \leq \hat{v}_{tri} \quad (4.4)$$

Let us assume (though this assumption is not necessary) that $v_{control}$ varies very little during a switching time period, that is, $m_f$ is large, as shown in Fig.4.6b. Therefore, assuming $v_{control}$ to be constant over a switching time period, Eq. (4.4) indicates how the "instantaneous average" value of $v_{ao}$ (averaged over one switching time period $T_s$) varies from one switching time period to the next. This "instantaneous average" is the same as the fundamental-frequency component of $v_{ao}$.

The foregoing argument shows why $v_{control}$ is chosen to be sinusoidal to provide a sinusoidal output voltage with fewer harmonics. Let the control voltage vary sinusoidally at the frequency $f_1 = \omega_1/2\pi$, which is the desired (or the fundamental) frequency of the inverter output:

$$v_{control} = \hat{v}_{control} \sin \omega_1 t$$

where

$$\hat{v}_{control} \leq \hat{v}_{tri} \quad (4.5)$$

Using Eqs. (4.4) and (4.5) and the foregoing arguments, which show that the fundamental-frequency component $(v_{ao})_1$ varies sinusoidally and in phase with $v_{control}$ as a function of time, results in

$$(v_{ao})_1 = \frac{\hat{v}_{control}}{\hat{v}_{tri}} \sin \omega_1 t \frac{V_d}{2} = m_a \sin \omega_1 t \frac{V_d}{2} \quad \text{for } m_a \leq 1 \quad (4.6)$$

Therefore,

$$\hat{(v_{ao})}_1 = m_a \frac{V_d}{2} \quad \text{for } m_a \leq 1 \quad (4.7)$$

which shows that in a sinusoidal PWM, the amplitude of the fundamental-frequency component of the output voltage varies linearly with $m_a$ (provided $m_a \leq 1.0$). Therefore, the range of $m_a$ from 0 to 1 is referred to as the linear range.
2. The harmonics in the inverter output voltage waveform appear as sidebands, centered around the switching frequency and its multiples, that is, around harmonics $m_f$, $2m_f$, $3m_f$, and so on. This general pattern holds true for all values of $m_a$ in the range 0 to 1.

For a frequency modulation ratio $m_f \leq 9$ (which is always the case, except in very high power ratings), the harmonic amplitudes are almost independent of $m_f$, though $m_f$ defines the frequencies at which they occur. Theoretically, the frequencies at which voltage harmonics occur can be indicated as:

$$f_h = \left(jm_f \pm k\right)f_1$$

that is, the harmonic order $h$ corresponds to the $k^{th}$ sideband of $j$ times the frequency modulation ratio $m_f$:

$$h = j\left(m_f\right)\pm k$$  \hspace{1cm} (4.8)

where the fundamental frequency corresponds to $h = 1$. For odd values of $j$, the harmonics exist only for even values of $k$. For even values of $j$, the harmonics exist only for odd values of $k$.

In Table 8-1, the normalized harmonics $(\hat{v}_{Ao})_h/\frac{1}{2}V_d$ are tabulated as a function of the amplitude modulation ratio $m_a$, assuming $m_f \geq 9$. Only those with significant amplitudes up to $j = 4$ in Eq.4.8 are shown.

It will be useful later on to recognize that in the inverter circuit of Fig.4.4

$$v_{AN} = v_{Ao} + \frac{1}{2}V_d$$  \hspace{1cm} (4.9)

Therefore, the harmonic voltage components in $v_{AN}$ and $v_{Ao}$ are the same:

$$(\hat{v}_{AN})_h = (\hat{v}_{Ao})_h$$  \hspace{1cm} (4.10)

Table 1 shows that Eq.7 is followed almost exactly and the amplitude of the fundamental component in the output voltage varies linearly with $m_a$.

3. The harmonic $m_f$ should be an odd integer. Choosing $m_f$ as an odd integer results in an odd symmetry as well as a half-wave symmetry with the time origin shown in Fig.4.5b, which is plotted for $m_f = 15$. Therefore, only odd harmonics are present and the even harmonics disappear from the waveform of $v_{Ao}$. Moreover, only the coefficients of the sine series in the Fourier analysis are finite; those for the cosine series are zero. The harmonic spectrum is plotted in Fig.4.5c.

Table 1 Generalized Harmonics of $v_{Ao}$, for a Large $m_f$
Example 1 In the circuit of Fig. 4.4, $V_d = 300V$, $m_d = 0.8$, $m_f = 39$, and the fundamental frequency is 47 Hz. Calculate the rms values of the fundamental-frequency voltage and some of the dominant harmonics in $v_{Ao}$ using Table 1.

Solution: From Table 1, the rms voltage at any value of $h$ is given as:

$$V_{(Ao)h} = \frac{1}{\sqrt{2}} \frac{V_d}{V_d/2} = 106.07 \frac{(V_{Ao})_h}{V_d/2} \tag{4.11}$$

Therefore, from Table 1 the rms voltages are as follows:

- Fundamental: $(V_{Ao})_1 = 106.07 \times 0.8 = 84.86 \text{ V}$ at 47 Hz
- $(V_{Ao})_{37} = 106.07 \times 0.22 = 23.33 \text{ V}$ at 1739 Hz
- $(V_{Ao})_{39} = 106.07 \times 0.818 = 86.76 \text{ V}$ at 1833 Hz
- $(V_{Ao})_{41} = 106.07 \times 0.22 = 23.33 \text{ V}$ at 1927 Hz
- $(V_{Ao})_{77} = 106.07 \times 0.314 = 33.31 \text{ V}$ at 3619 Hz
- $(V_{Ao})_{79} = 106.07 \times 0.314 = 33.31 \text{ V}$ at 3713 Hz

Therefore, from Table 1 the rms voltages are as follows:

<table>
<thead>
<tr>
<th>$h$</th>
<th>$m_a$</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$m_f$</td>
<td>1.242</td>
<td>1.15</td>
<td>1.006</td>
<td>0.818</td>
<td>0.601</td>
</tr>
<tr>
<td>2</td>
<td>$m_f \pm 2$</td>
<td>0.016</td>
<td>0.061</td>
<td>0.131</td>
<td>0.220</td>
<td>0.318</td>
</tr>
<tr>
<td>3</td>
<td>$m_f \pm 4$</td>
<td>0.018</td>
<td>0.014</td>
<td>0.013</td>
<td>0.013</td>
<td></td>
</tr>
</tbody>
</table>

Note: $(V_{Ao})_h/\sqrt{2} (V_{Ao})_h/\sqrt{2}$ is tabulated as a function of $m_a$.

Now we discuss the selection of the switching frequency and the frequency modulation ratio $m_f$. Because of the relative ease in filtering harmonic voltages at high frequencies, it is desirable to use as high a switching frequency as possible, except for one significant drawback: Switching losses in the inverter switches increase proportionally with the switching frequency $f_s$. Therefore, in most applications, the switching frequency is selected to be either less than 6 kHz or greater than 20 kHz to be above the audible range. If the optimum switching frequency (based on the overall system performance) turns out to be somewhere in the 6-20-kHz range, then the disadvantages of increasing it to 20 kHz are often outweighed by the advantage of no audible noise with $f_s$ of 20 kHz or greater. Therefore, in 50- or 60-Hz type applications, such as ac motor drives (where the fundamental frequency of the inverter output may be required to be as high as 200 Hz), the frequency modulation ratio $m_f$ may be 9 or even less for switching frequencies of less than 2 kHz. On the other hand, $m_f$ will be larger than 100 for switching frequencies higher than 20 kHz. The desirable relationships between the triangular waveform signal and the control voltage signal are dictated by how large $m_f$ is. In the discussion here, $m_f = 21$ is treated as the borderline between large and small, though its selection is somewhat arbitrary. Here, it is assumed that the amplitude modulation ratio $m_d$ is less than 1.
4.2.1.1 Small \( m_f (m_f \leq 21) \)

1. Synchronous PWM. For small values of \( m_f \), the triangular waveform signal and the control signal should be synchronized to each other (synchronous PWM) as shown in Fig.4.5a. This synchronous PWM requires that \( m_f \) be an integer. The reason for using the synchronous PWM is that the asynchronous PWM (where \( m_f \) is not an integer) results in subharmonics (of the fundamental frequency) that are very undesirable in most applications. This implies that the triangular waveform frequency varies with the desired inverter frequency (e.g., if the inverter output frequency and hence the frequency of \( v_{\text{control}} \), is 65.42 Hz and \( m_f = 15 \), the triangular wave frequency should be exactly 15 \( \times \) 65.42 = 981.3 Hz).

2. \( m_f \) should be an odd integer. As discussed previously, \( m_f \) should be an odd integer except in single-phase inverters with PWM unipolar voltage switching, to be discussed in the following sections.

4.2.1.2 Large \( m_f (m_f > 21) \)

The amplitudes of subharmonics due to asynchronous PWM are small at large values of \( m_f \). Therefore, at large values of \( m_f \), the asynchronous PWM can be used where the frequency of the triangular waveform is kept constant, whereas the frequency of \( v_{\text{control}} \) varies, resulting in noninteger values of \( m_f \) (so long as they are large). However, if the inverter is supplying a load such as an ac motor, the subharmonics at zero or close to zero frequency, even though small in amplitude, will result in large currents that will be highly undesirable. Therefore, the asynchronous PWM should be avoided.

4.2.1.3 Overmodulation \( m_a > 1.0 \)

In the previous discussion, it was assumed that \( m_a \leq 1.0 \), corresponding to a sinusoidal PWM in the linear range. Therefore, the amplitude of the fundamental-frequency voltage varies linearly with \( m_a \), as derived in Eq.(4.7). In this range of \( m_a \leq 1.0 \), PWM pushes the harmonics into a high-frequency range around the switching frequency and its multiples. In spite of this desirable feature of a sinusoidal PWM in the linear range, one of the drawbacks is that the maximum available amplitude of the fundamental-frequency component is not as high as we wish. This is a natural consequence of the notches in the output voltage waveform of Fig.4.5b.

To increase further the amplitude of the fundamental-frequency component in the output voltage, \( m_a \) is increased beyond 1.0, resulting in what is called overmodulation. Overmodulation causes the output voltage to contain many more harmonics in the sidebands as compared with the linear range (with \( m_a \leq 1.0 \)), as shown in Fig.4.7. The harmonics with dominant amplitudes in the linear range may not be dominant during overmodulation. More significantly, with overmodulation, the amplitude of the fundamental-frequency component does not vary linearly with the amplitude modulation ratio \( m_a \). Figure 4.8 shows the normalized peak amplitude of the fundamental-frequency component \( \left( \hat{v}_{A_o} \right)_h / \frac{1}{2} V_d \) as a function of the amplitude modulation ratio \( m_a \). Even at reasonably large values of \( m_f \), \( \left( \hat{v}_{A_o} \right)_h / \frac{1}{2} V_d \) depends on \( m_f \) in the overmodulation region. This is contrary to the linear range \( (m_a \leq 1.0) \) where \( \left( \hat{v}_{A_o} \right)_h / \frac{1}{2} V_d \) varies linearly with \( m_a \), almost independent of \( m_f \) (provided \( m_f > 9 \)).
With overmodulation regardless of the value of $m_f$, it is recommended that a synchronous PWM operation be used, thus meeting the requirements indicated previously for a small value of $m_f$.

![Fig.4.7 Harmonics due to overmodulation, drawn for $m_a = 2.5$ and $m_f = 15$.](image)

![Fig.4.8 Voltage control by varying $m_a$.](image)

The overmodulation region is avoided in uninterruptible power supplies because of a stringent requirement on minimizing the distortion in the output voltage. In induction motor drives, overmodulation is normally used.

For sufficiently large values of $m_a$, the inverter voltage waveform degenerates from a pulse-width-modulated waveform into a square wave, which is discussed in detail in the next section. From Fig.4.8 and the discussion of square-wave switching to be presented in the next section, it can be concluded that in the overmodulation region with $m_a > 1$

\[
\frac{V_d}{2} < \left( \hat{V}_{Ao} \right)_h < \frac{4}{\pi} \frac{V_d}{2}
\]

(4.12)

### 4.2.2 SQUARE-WAVE SWITCHING SCHEME

In the square-wave switching scheme, each switch of the inverter leg of Fig.4.4 is on for one half-cycle ($180^\circ$) of the desired output frequency. This results in an output voltage waveform as shown in
Fig.4.9a. From Fourier analysis, the peak values of the fundamental-frequency and harmonic components in the inverter output waveform can be obtained for a given input $V_d$ as:

$$
(\hat{V}_{A0})_h = \frac{4V_d}{\pi} = 1.273 \left(\frac{V_d}{2}\right)
$$

(4.13)

and

$$
(\hat{V}_{A0})_h = \frac{(\hat{V}_{A0})_1}{h}
$$

(4.14)

where the harmonic order $h$ takes on only odd values, as shown in Fig.4.9b. It should be noted that the square-wave switching is also a special case of the sinusoidal PWM switching when $m_a$ becomes so large that the control voltage waveform intersects with the triangular waveform in Fig.4.5a only at the zero crossing of $v_{control}$. Therefore, the output voltage is independent of $m_a$ in the square-wave region, as shown in Fig.4.8.

One of the advantages of the square-wave operation is that each inverter switch changes its state only twice per cycle, which is important at very high power levels where the solid-state switches generally have slower turn-on and turn-off speeds. One of the serious disadvantages of square-wave switching is that the inverter is not capable of regulating the output voltage magnitude. Therefore, the dc input voltage $V_d$ to the inverter must be adjusted in order to control the magnitude of the inverter output voltage.

**4.3 SINGLE PHASE INVERTERS**

**4.3.1 HALF-BRIDGE INVERTERS (SINGLE PHASE)**

Figure 4.10 shows the half-bridge inverter. Here, two equal capacitors are connected in series across the dc input and their junction is at a midpotential, with a voltage $\frac{1}{2}V_d$, across each capacitor.

Sufficiently large capacitances should be used such that it is reasonable to assume that the potential at point o remains essentially constant with respect to the negative dc bus N. Therefore, this circuit configuration is identical to the basic one-leg inverter discussed in detail earlier, and $v_o = v_{A0}$.

Assuming PWM switching, we find that the output voltage waveform will be exactly as in Fig.4.5b. It should be noted that regardless of the switch states, the current between the two capacitors C+ and C- (which have equal and very large values) divides equally. When $T^+$ is on, either $T^+$ or $D^+$ conducts depending on the direction of the output current, and $i_o$ splits equally between the two capacitors. Similarly, when the switch $T^-$ is in its on state, either $T^-$ or $D^-$ conducts depending on the direction of $i_o$, and $i_o$ splits equally between the two capacitors. Therefore, the capacitors C+ and C- are "effectively" connected in parallel in the path of $i_o$. This also explains why the junction o in Fig.4.10 stays at midpotential.

Since $i_o$ must flow through the parallel combination of C+ and C-, $i_o$ in steady state cannot have a dc component. Therefore, these capacitors act as dc blocking capacitors, thus eliminating the problem of transformer saturation from the primary side, if a transformer is used at the output to provide
electrical isolation. Since the current in the primary winding of such a transformer would not be forced to zero with each switching, the transformer leakage inductance energy does not present a problem to the switches.

In a half-bridge inverter, the peak voltage and current ratings of the switches are as follows:

\[ V_T = V_d \]  \hspace{1cm} (4.15)

and \[ I_T = i_{o,\text{peak}} \]  \hspace{1cm} (4.16)

### 4.3.2 FULL-BRIDGE INVERTERS (SINGLE PHASE)

A full-bridge inverter is shown in Fig.4.11. This inverter consists of two one-leg inverters of the type discussed in Section 4-2 and is preferred over other arrangements in higher power ratings. With the same dc input voltage, the maximum output voltage of the full-bridge inverter is twice that of the half-bridge inverter. This implies that for the same power, the output current and the switch currents are one-half of those for a half-bridge inverter. At high power levels, this is a distinct advantage, since it requires less paralleling of devices.

![Fig.4.10 Half-bridge inverter.](image)

![Fig.4.11 Single-phase full-bridge inverter.](image)

#### 4.3.2.1 PWM with Bipolar Voltage Switching

The diagonally opposite switches \((T_{A+}, T_{B-})\) and \((T_{A-}, T_{B+})\) from the two legs in Fig.4.11 are switched as switch pairs 1 and 2, respectively. With this type of PWM switching, the output voltage waveform of leg A is identical to the output of the basic one-leg inverter, which is determined in the same manner by comparison of \(v_{\text{control}}\) and \(v_{\text{tri}}\) in Fig.4.12a. The output of inverter leg B is negative of the leg A output; for example, when \(T_{A+}\) is on and \(v_{A0}\) is equal to \(+\frac{1}{2}V_d\) is also on and \(v_{B0} = -\frac{1}{2}V_d\). Therefore:

\[ v_{B0}(t) = -v_{A0}(t) \]  \hspace{1cm} (4.17)

and \[ v_o(t) = v_{A0}(t) - v_{B0}(t) = 2v_{A0}(t) \]  \hspace{1cm} (4.18)

The \(v_o\) waveform is shown in Fig.4.12b. The analysis carried out in Section 4.2 for the basic one-leg inverter completely applies to this type of PWM switching. Therefore, the peak of the fundamental-frequency component in the output voltage \(\dot{V}_{o1}\) can be obtained from Eqs. (4.7), (4.12), and (4.18) as:
\[ \hat{V}_{o1} = m_a V_d \quad (m_a \leq 1.0) \]  

and \[ V_d < \hat{V}_{o1} < \frac{4}{\pi} V_d \quad (m_a > 1.0) \]  

(4.19)  

(4.20).

In Fig.4.12b, we observe that the output voltage \( v_o \) switches between \( -V_d \) and \( +V_d \) voltage levels. That is the reason why this type of switching is called a PWM with bipolar voltage switching. The amplitudes of harmonics in the output voltage can be obtained by using Table 1, as illustrated by the following example.

**Example 2** In the full-bridge converter circuit of Fig.4.11, \( V_d = 300V \), \( m_a = 0.8 \), \( m_f = 39 \), and the fundamental frequency is 47 Hz. Calculate the rms values of the fundamental-frequency voltage and some of the dominant harmonics in the output voltage \( v_o \) if a PWM bipolar voltage-switching scheme is used.

**Solution:** From Eq.(4.18), the harmonics in \( v_o \) can be obtained by multiplying the harmonics in Table 1 and **Example 1** by a factor of 2. Therefore from Eq. (4.11), the rms voltage at any harmonic \( h \) is given as

\[
(V_o)_h = \frac{1}{\sqrt{2}} \times 2 \times \frac{V_d}{2} \times \frac{(\hat{V}_{Ao})_h}{V_d/2} = 212.13 \times \frac{(\hat{V}_{Ao})_h}{V_d/2} \quad (4.21)
\]

Therefore, the rms voltages are as follows:

**Fundamental:** \( V_{o1} = 212.13 \times 0.8 = 169.7 \) V at 47 Hz  
\( (V_o)_{37} = 212.13 \times 0.22 = 46.67 \) V at 1739 Hz  
\( (V_o)_{39} = 212.13 \times 0.818 = 173.52 \) V at 1833 Hz  
\( (V_o)_{41} = 212.13 \times 0.22 = 46.67 \) V at 1927 Hz  
\( (V_o)_{77} = 212.13 \times 0.314 = 66.60 \) V at 3619 Hz  
\( (V_o)_{79} = 212.13 \times 0.314 = 66.60 \) V at 3713 Hz  

etc.

**dc-Side Current** \( i_d \) It is informative to look at the dc-side current \( i_d \) in the PWM biopolar voltage-switching scheme.

For simplicity, fictitious L-C high-frequency filters will be used at the dc side as well as at the ac side, as shown in Fig.4.13. The switching frequency is assumed to be very high, approaching infinity. Therefore, to filter out the high-switching-frequency components in \( v_o \) and \( i_d \), the filter components L
and C required in both ac and dc-side filters approach zero. This implies that the energy stored in the filters is negligible. Since the converter itself has no energy storage elements, the instantaneous power input must equal the instantaneous power output.

![Fig.4.13 Inverter with "fictitious" filters.](Image)

Having made these assumptions, \( v_o \) in Fig. 4.13 is a pure sine wave at the fundamental output frequency \( \omega_1 \).

\[
v_{o1} = v_o = \sqrt{2} V_o \sin \omega_1 t \tag{4.22}
\]

If the load is as shown in Fig. 4.13, where \( e_o \) is a sine wave at frequency \( \omega_1 \), then the output current would also be sinusoidal and would lag \( v_o \) for an inductive load such as an ac motor:

\[
io = \sqrt{2} I_o \sin \left(\sqrt{\omega_1} t - \phi\right) \tag{4.23}
\]

where \( \phi \) is the angle by which \( i_o \) lags \( v_o \).

On the dc side, the L-C filter will filter the high-switching-frequency components in \( i_d \) and \( i_d^* \) would only consist of the low-frequency and dc components. Assuming that no energy is stored in the filters,

\[
V_d i_d^*(t) = v_o(t)i_o(t) = \sqrt{2} V_o \sin \omega_1 t \sqrt{2} I_o \sin \left(\omega_1 t - \phi\right) \tag{4.24}
\]

Therefore

\[
i_d^*(t) = \frac{V_o I_o}{V_d} \cos \phi - \frac{V_o I_o}{V_d} \cos \left(2 \omega_1 t - \phi\right) = I_d + i_{d2} \tag{4.25}
\]

\[
i_d^*(t) = I_d - \sqrt{2} I_{d2} \cos \left(2 \omega_1 t - \phi\right) \tag{4.26}
\]

where

\[
I_d = \frac{V_o I_o}{V_d} \cos \phi \tag{4.27}
\]

and

\[
i_{d2} = \frac{1}{\sqrt{2}} \frac{V_o I_o}{V_d} \tag{4.28}
\]

Equation (4.26) for \( i_d^* \) shows that it consists of a dc component \( I_d \), which is responsible for the power transfer from \( V_d \) on the dc side of the inverter to the ac side. Also, \( i_d^* \) contains a sinusoidal component at twice the fundamental frequency. The inverter input current \( i_d \) consists of \( i_d^* \) and the high-frequency components due to inverter switchings, as shown in Fig. 4.14.
In practical systems, the previous assumption of a constant dc voltage as the input to the inverter is not entirely valid. Normally, this dc voltage is obtained by rectifying the ac utility line voltage. A large capacitor is used across the rectifier output terminals to filter the dc voltage. The ripple in the capacitor voltage, which is also the dc input voltage to the inverter, is due to two reasons: (1) The rectification of the line voltage to produce dc does not result in a pure dc, dealing with the line-frequency rectifiers. (2) As shown earlier by Eq.(4.26), the current drawn by a single-phase inverter from the dc side is not a constant dc but has a second harmonic component (of the fundamental frequency at the inverter output) in addition to the high switching-frequency components. The second harmonic current component results in a ripple in the capacitor voltage, although the voltage ripple due to the high switching frequencies is essentially negligible.

4.3.2.2 PWM with Unipolar Voltage Switching

In PWM with unipolar voltage switching, the switches in the two legs of the full-bridge inverter of Fig.4.11 are not switched simultaneously, as in the previous PWM scheme. Here, the legs A and B of the full-bridge inverter are controlled separately by comparing \( v_{\text{tri}} \) with \( v_{\text{control}} \) and \( -v_{\text{control}} \), respectively. As shown in Fig.4.15a, the comparison of \( v_{\text{control}} \) with the triangular waveform results in the following logic signals to control the switches in leg A:

\[
\begin{align*}
& v_{\text{control}} > v_{\text{tri}} \quad T_{A+} \text{ on} \quad \text{and} \quad V_{AN} = V_d \\
& v_{\text{control}} < v_{\text{tri}} \quad T_{A-} \text{ on} \quad \text{and} \quad V_{AN} = 0
\end{align*}
\]

The output voltage of inverter leg A with respect to the negative dc bus N is shown in Fig.4.15b. For controlling the leg B switches, \(-v_{\text{control}}\) is compared with the same triangular waveform, which yields the following:

\[
\begin{align*}
& -v_{\text{control}} > v_{\text{tri}} \quad T_{B+} \text{ on} \quad \text{and} \quad V_{BN} = V_d \\
& -v_{\text{control}} < v_{\text{tri}} \quad T_{B-} \text{ on} \quad \text{and} \quad V_{BN} = 0
\end{align*}
\]

Because of the feedback diodes in antiparallel with the switches, the foregoing voltages given by Eqs.(4.29) and (4.30) are independent of the direction of the output current \( i_o \).

The waveforms of Fig.4.15 show that there are four combinations of switch on-states and the corresponding voltage levels:

1. \( T_{A+}, T_{B-} \) on: \( v_{AN} = V_d, \quad v_{BN} = 0; \quad v_o = V_d \)
2. \( T_{A-}, T_{B+} \) on: \( v_{AN} = 0, \quad v_{BN} = V_d; \quad v_o = -V_d \)
3. \( T_{A+}, T_{B+} \) on: \( v_{AN} = V_d, \quad v_{BN} = V_d; \quad v_o = 0 \)
4. \( T_{A-}, T_{B-} \) on: \( v_{AN} = 0, \quad v_{BN} = 0; \quad v_o = 0 \)

\[ (4.31) \]
We notice that when both the upper switches are on, the output voltage is zero. The output current circulates in a loop through $T_{A+}$ and $D_{B+}$ or $D_{A+}$ and $T_{B+}$ depending on the direction of $i_o$. During this interval, the input current $i_d$ is zero. A similar condition occurs when both bottom switches $T_{A-}$ and $T_{B-}$ are on.

In this type of PWM scheme, when a switching occurs, the output voltage changes between zero and $+V_d$ or between zero and $-V_d$ voltage levels. For this reason, this type of PWM scheme is called PWM with a unipolar voltage switching, as opposed to the PWM with bipolar (between $+V_d$ and $-V_d$) voltage-switching scheme described earlier. This scheme has the advantage of "effectively" doubling the switching frequency as far as the output harmonics are concerned, compared to the bipolar voltage switching scheme. Also, the voltage jumps in the output voltage at each switching are reduced to $V_d$ as compared to $2V_d$ in the previous scheme.

The advantage of "effectively" doubling the switching frequency appears in the harmonic spectrum of the output voltage waveform, where the lowest harmonics (in the idealized circuit) appear as sidebands of twice the switching frequency. It is easy to understand this if we choose the frequency modulation ratio $m_f$ to be even ($m_f$ should be odd for PWM with bipolar voltage switching) in a single-phase inverter. The voltage waveforms $v_{AN}$ and $v_{BN}$ are displaced by $180^\circ$ of the fundamental frequency $f_1$ with respect to each other. Therefore, the harmonic components at the switching frequency in $v_{AN}$ and $v_{BN}$ have the same phase ($\phi_{AN} - \phi_{BN} = 180^\circ.m_f = 0$, since the waveforms are
180° displaced and \( m_f \) is assumed to be even). This results in the cancellation of the harmonic component at the switching frequency in the output voltage \( V_o = V_{AN} - V_{BN} \). In addition, the sidebands of the switching-frequency harmonics disappear. In a similar manner, the other dominant harmonic at twice the switching frequency cancels out, while its sidebands do not. Here also

\[
\hat{V}_{o1} = m_a V_d \quad (m_a \leq 1.0) \\
\text{and} \quad V_d < \hat{V}_{o1} < \frac{4}{\pi} V_d \quad (m_a > 1.0)
\] (4.32)

**Example 3** In **Example 2**, suppose that a PWM with unipolar voltage switching scheme is used, with \( m_f = 38 \). Calculate the rms values of the fundamental frequency voltage and some of the dominant harmonics in the output voltage.

**Solution:** Based on the discussion of unipolar voltage switching, the harmonic order \( h \) can be written as

\[
h = j(2m_f) \pm k
\] (4.34)

where the harmonics exist as sidebands around \( 2m_f \) and the multiples of \( 2m_f \). Since \( h \) is odd, \( k \) in Eq.(34) attains only odd values. From **Example 2**,

\[
(V_o)_h = 212.13 \left(\frac{V_{d0}}{V_d}\right)_h
\] (4.35)

Using Eq.(35) and Table 1, we find that the rms voltages are as follows:

- At fundamental or 47 Hz: \( V_{o1} = 0.8 \times 212.13 = 169.7 \text{ V} \)
- At \( h = 2m_f - 1 = 75 \) or 3525 Hz: \( (V_o)_{75} = 0.314 \times 212.13 = 66.60 \text{ V} \)
- At \( h = 2m_f + 1 = 77 \) or 3619 Hz: \( (V_o)_{77} = 0.314 \times 212.13 = 66.60 \text{ V} \) etc.

Comparison of the unipolar voltage switching with the bipolar voltage switching of **Example 2** shows that, in both cases, the fundamental-frequency voltages are the same for equal \( m_d \). However, with unipolar voltage switching, the dominant harmonic voltages centered around \( m_f \) disappear, thus resulting in a significantly lower harmonic content.

**dc-Side Current** \( i_d \). Under conditions similar to those in the circuit of Fig 4.13 for the PWM with bipolar voltage switching, Fig. 4.16 shows the dc-side current \( i_d \) for the PWM unipolar voltage-switching scheme, where \( m_f = 14 \) (instead of \( m_f = 15 \) for the bipolar voltage switching).

By comparing Figs. 4.14 and 4.16, it is clear that using PWM with unipolar voltage switching results in a smaller ripple in the current on the dc side of the inverter.

![Fig.4.16 The dc-side current in a single-phase inverter with PWM unipolar voltage switching.](image)

**4.3.2.3 Square-Wave Operation**
The full-bridge inverter can also be operated in a square-wave mode. Both types of PWM discussed earlier degenerate into the same square-wave mode of operation, where the switches \((T_{A+}, T_{B-})\) and \((T_{B+}, T_{A-})\) are operated as two pairs with a duty ratio of 0.5.

As is the case in the square-wave mode of operation, the output voltage magnitude given below is regulated by controlling the input dc voltage:

\[
\hat{V}_{ol} = \frac{4}{\pi} V_d
\]  

(4.36)

### 4.3.2.4 Output Control by Voltage Cancellation

This type of control is feasible only in a single-phase, full-bridge inverter circuit. It is based on the combination of square-wave switching and PWM with a unipolar voltage switching. In the circuit of Fig.4.17a, the switches in the two inverter legs are controlled separately (similar to PWM unipolar voltage switching). But all switches have a duty ratio of 0.5, similar to a square-wave control. This results in waveforms for \(v_{AN}\) and \(v_{BN}\) shown in Fig.4.17b, where the waveform overlap angle \(\alpha\) can be controlled. During this overlap interval, the output voltage is zero as a consequence of either both top switches or both bottom switches being on. With \(\alpha = 0\), the output waveform is similar to a square-wave inverter with the maximum possible fundamental output magnitude.

![Fig.17 Full-bridge single-phase inverter control by voltage cancellation: (a) power circuit; (b) waveforms; (c) normalized fundamental and harmonic voltage output and total harmonic distortion as a function of \(\alpha\).](image)

It is easier to derive the fundamental and the harmonic frequency components of the output voltage in terms of \(\beta = 90^\circ - \frac{1}{2} \alpha\), as is shown in Fig.4.17b:

\[
(\hat{V}_o)_h = \frac{2}{\pi} \int_{-\pi/2}^{\pi/2} v_o \cos(h\theta) \, d\theta
= \frac{2}{\pi} \int_{-\beta}^{\beta} V_d \cos(h\theta) \, d\theta
= \frac{4}{\pi h} V_d \sin(h\beta)
\]

(4.37)

where \(\beta = 90^\circ - \frac{1}{2} \alpha\) and \(h\) is an odd integer.
Fig.4.17c shows the variation in the fundamental-frequency component as well as the harmonic voltages as a function of $\alpha$. These are normalized with respect to the fundamental-frequency component for the square-wave ($\alpha = 0$) operation. The total harmonic distortion, which is the ratio of the rms value of the harmonic distortion to the rms value of the fundamental-frequency component, is also plotted as a function of $\alpha$. Because of a large distortion, the curves are shown as dashed for large values of $\alpha$.

### 4.3.2.5 Switch Utilization in Full-Bridge Inverters

Similar to a half-bridge inverter, if a transformer is utilized at the output of a full-bridge inverter, the transformer leakage inductance does not present a problem to the switches.

Independent of the type of control and the switching scheme used, the peak switch voltage and current ratings required in a full-bridge inverter are as follows:

\[ V_T = V_d \] (4.38)
\[ I_T = i_o, \text{peak} \] (4.39)

### 4.3.2.6 Ripple in the Single-Phase Inverter Output

The ripple in a repetitive waveform refers to the difference between the instantaneous values of the waveform and its fundamental-frequency component.

Fig.4.18a shows a single-phase switch-mode inverter. It is assumed to be supplying an induction motor load, which is shown by means of a simplified equivalent circuit with a counter electromotive force (emf) $e_o$. Since $e_o(t)$ is sinusoidal, only the sinusoidal (fundamental-frequency) components of the inverter output voltage and current are responsible for the real power transfer to the load.

We can separate the fundamental-frequency and the ripple components in $v_o$ and $i_o$ by applying the principle of superposition to the linear circuit of Fig.4.18a. Let $v_o = v_{o1} + v_{\text{ripple}}$ and $i_o = i_{o1} + i_{\text{ripple}}$. Figs.4.18b, c show the circuits at the fundamental frequency and at the ripple frequency, respectively, where the ripple frequency component consists of sub-components at various harmonic frequencies.

Therefore, in a phasor form (with the fundamental frequency components designated by subscript 1) as shown in Fig.4.18d,

\[ V_{o1} = E_o + V_{L1} = E_o + j\omega_L I_{o1} \] (4.40)

![Fig.4.18 Single-phase inverter: (a) circuit; (b) fundamental-frequency components; (c) ripple frequency components; (d) fundamental-frequency phasor diagram.](image-url)
Since the superposition principle is valid here, all the ripple in \( v \), appears across \( L \), where
\[
v_{\text{ripple}}(t) = v_o - v_{o1} \quad (4.41)
\]
The output current ripple can be calculated as
\[
i_{\text{ripple}}(t) = \frac{1}{L} \int_0^t v_{\text{ripple}}(\zeta) d\zeta + k \quad (4.42)
\]
where \( k \) is a constant and \( \zeta \) is a variable of integration.

With a properly selected time origin \( t = 0 \), the constant \( k \) in Eq.(4.42) will be zero. Therefore, Eqs.(4.41) and (4.42) show that the current ripple is independent of the power being transferred to the load.

As an example, Fig.4.19a shows the ripple current for a square-wave inverter output. Fig.4.19b shows the ripple current in a PWM bipolar voltage switching. In drawing Figs.4.19a and 4.19b, the fundamental-frequency components in the inverter output voltages are kept equal in magnitude (this requires a higher value of \( V_d \) in the PWM inverter). The PWM inverter results in a substantially smaller peak ripple current compared to the square-wave inverter. This shows the advantage of pushing the harmonics in the inverter output voltage to as high frequencies as feasible, thereby reducing the losses in the load by reducing the output current harmonics. This is achieved by using higher inverter switching frequencies, which would result in more frequent switching and hence higher switching losses in the inverter. Therefore, from the viewpoint of the overall system energy efficiency, a compromise must be made in selecting the inverter switching frequency.

![Fig. 4.19 Ripple in the inverter output: (a) square-wave switching; (b) PWM bipolar voltage switching.](image)

### 4.3.3 PUSH-PULL INVERTERS

Fig.4.20 shows a push-pull inverter circuit. It requires a transformer with a center tapped primary. We will initially assume that the output current \( i_o \) flows continuously. With this assumption, when the switch \( T_1 \) is on (and \( T_2 \) is off), \( T_1 \) would conduct for a positive value of \( i_o \), and \( D_1 \) would conduct for a negative value of \( i_o \). Therefore, regardless of the direction of \( i_o \), \( v_o = V_d / n \), where \( n \) is the transformer turns ratio between the primary half and the secondary windings, as shown in Fig.4.20. Similarly, when \( T_2 \) is on (and \( T_1 \) is off), \( v_o = -V_d / n \). A push-pull inverter can be operated in a PWM or a square-wave mode and the waveforms are identical to those in Figs.4.5 and 4.12 for half-bridge and full-bridge inverters. The output voltage in Fig.4.20 equals:
\[
\hat{V}_{o1} = m_a \frac{V_d}{n} \quad (m_a \leq 1.0)
\]

and
\[
\frac{V_d}{n} < \hat{V}_{o1} < \frac{4V_d}{\pi n} \quad (m_a > 1.0)
\]

In a push-pull inverter, the peak switch voltage and current ratings are
\[
V_T = 2V_d \quad I_T = i_{o,peak}/n
\]

Fig.4.20 Push-Pull inverter (single phase).

The main advantage of the push-pull circuit is that no more than one switch in series conducts at any instant of time. This can be important if the dc input to the converter is from a low-voltage source, such as a battery, where the voltage drops across more than one switch in series would result in a significant reduction in energy efficiency. Also, the control drives for the two switches have a common ground. It is, however, difficult to avoid the dc saturation of the transformer in a push-pull inverter.

The output current, which is the secondary current of the transformer, is a slowly varying current at the fundamental output frequency. It can be assumed to be a constant during a switching interval. When a switching occurs, the current shifts from one half to the other half of the primary winding. This requires very good magnetic coupling between these two half-windings in order to reduce the energy associated with the leakage inductance of the two primary windings. This energy will be dissipated in the switches or in snubber circuits used to protect the switches. This is a general phenomenon associated with all converters (or inverters) with isolation where the current in one of the windings is forced to go to zero with every switching. This phenomenon is very important in the design of such converters.

In a pulse-width-modulated push-pull inverter for producing sinusoidal output (unlike those used in switch-mode dc power supplies), the transformer must be designed for the fundamental output frequency. The number of turns will therefore be high compared to a transformer designed to operate at the switching frequency in a switch-mode dc power supply. This will result in a high transformer leakage inductance, which is proportional to the square of the number of turns, provided all other dimensions are kept constant. This makes it difficult to operate a sine-wave-modulated PWM push-pull inverter at switching frequencies higher than approximately 1 kHz.

### 4.3.4 SWITCH UTILIZATION IN SINGLE-PHASE INVERTERS

Since the intent in this section is to compare the utilization of switches in various single-phase inverters, the circuit conditions are idealized. We will assume that \( V_{d,\text{max}} \) is the highest value of the input voltage, which establishes the switch voltage ratings. In the PWM mode, the input remains constant at \( V_{d,\text{max}} \). In the square-wave mode, the input voltage is decreased below \( V_{d,\text{max}} \) to decrease the output voltage from its maximum value. Regardless of the PWM or the square-wave mode of operation, we assume that there is enough inductance associated with the output load to yield a purely sinusoidal current (an idealized condition indeed for a square-wave output) with an rms value of \( I_{o,\text{max}} \) at the maximum load.
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If the output current is assumed to be purely sinusoidal, the inverter rms volt-ampere output at the fundamental frequency equals \( V_{o1}I_{o,\text{max}} \) at the maximum rated output, where the subscript 1 designates the fundamental-frequency component of the inverter output. With \( V_T \) and \( I_T \) as the peak voltage and current ratings of a switch, the combined utilization of all the switches in an inverter can be defined as

\[
\text{Switch utilization ratio} = \frac{V_{o1}I_{o,\text{max}}}{q V_T I_T} \tag{4.46}
\]

where \( q \) is the number of switches in an inverter.

To compare the utilization of switches in various single-phase inverters, we will initially compare them for a square-wave mode of operation at the maximum rated output. (The maximum switch utilization occurs at \( V_d = V_{d,\text{max}} \)).

**Push–Pull Inverter**

\[
V_T = 2V_{d,\text{max}}, \quad I_T = \sqrt{2} \frac{I_{o,\text{max}}}{n}, \quad V_{o1,\text{max}} = \frac{4}{\pi \sqrt{2}} \frac{V_{d,\text{max}}}{n}, \quad q = 2 \tag{8-47}
\]

(\( n = \) turns ratio, Fig. 8-20)

\[
\therefore \text{Maximum switch utilization ratio} = \frac{1}{2\pi} \approx 0.16 \tag{8-48}
\]

**Half-Bridge Inverter**

\[
V_T = V_{d,\text{max}}, \quad I_T = \sqrt{2} I_{o,\text{max}}, \quad V_{o1,\text{max}} = \frac{4}{\pi \sqrt{2}} \frac{V_{d,\text{max}}}{2}, \quad q = 2 \tag{8-49}
\]

\[
\therefore \text{Maximum switch utilization ratio} = \frac{1}{2\pi} \approx 0.16 \tag{8-50}
\]

**Full-Bridge Inverter**

\[
V_T = V_{d,\text{max}}, \quad I_T = \sqrt{2} I_{o,\text{max}}, \quad V_{o1,\text{max}} = \frac{4}{\pi \sqrt{2}} V_{d,\text{max}}, \quad q = 4 \tag{8-51}
\]

\[
\therefore \text{Maximum switch utilization ratio} = \frac{1}{2\pi} \approx 0.16 \tag{8-52}
\]

This shows that in each inverter, the switch utilization is the same with

\[
\text{Maximum switch utilization ratio} = \frac{1}{2\pi} \approx 0.16 \tag{8-53}
\]

In practice, the switch utilization ratio would be much smaller than 0.16 for the following reasons: (1) switch ratings are chosen conservatively to provide safety margins; (2) in determining the switch current rating in a PWM inverter, one would have to take into account the variations in the input dc voltage available; and (3) the ripple in the output current would influence the switch current rating. Moreover, the inverter may be required to supply a short-term overload. Thus, the switch utilization ratio, in practice, would be substantially less than the 0.16 calculated.

At the lower output volt-amperes compared to the maximum rated output, the switch utilization decreases linearly. It should be noted that using a PWM switching with \( mp \approx 1.0 \), this ratio would be smaller by a factor of \((\pi / 4)m_a\) as compared to the square-wave switching:

\[
\text{Maximum switch utilization ratio} = \frac{1}{2\pi} \frac{\pi}{4} m_a = \frac{1}{8} m_a, \quad m_a \leq 1.0 \tag{4.54}
\]

Therefore, the theoretical maximum switch utilization ratio in a PWM switching is only 0.125 at \( m_a = 1 \), as compared with 0.16 in square–wave inverter.
Example 4 In a single-phase full-bridge PWM inverter, \( V_d \) varies in a range of 295-325 V. The output voltage is required to be constant at 200 V (rms), and the maximum load current (assumed to be sinusoidal) is 10 A (rms). Calculate the combined switch utilization ratio (under these idealized conditions, not accounting for any overcurrent capabilities).

Solution: In this inverter

\[
V_T = V_{d,ma} = 325 \text{V}
\]

\[
I_T = \sqrt{2}I_o = \sqrt{2} \times 10 = 14.14
\]

\[q = \text{no. of switches} = 4\]

The maximum output volt-ampere (fundamental frequency) is

\[V_o I_{o,\text{max}} = 200 \times 10 = 2000 \text{VA}\]  \hspace{1cm} (4.55)

Therefore, from Eq.(4.46)

\[
\text{Switch utilization ratio} = \frac{V_o I_{o,\text{max}}}{qV_T I_T} = \frac{2000}{4 \times 325 \times 14.14} = 0.11
\]

4.4 THREE-PHASE INVERTERS

In applications such as uninterruptible ac power supplies and ac motor drives, three-phase inverters are commonly used to supply three-phase loads. It is possible to supply a three-phase load by means of three separate single-phase inverters, where each inverter produces an output displaced by 120° (of the fundamental frequency) with respect to each other. Though this arrangement may be preferable under certain conditions, it requires either a three-phase output transformer or separate access to each of the three phases of the load. In practice, such access is generally not available. Moreover, it requires 12 switches.

The most frequently used three-phase inverter circuit consists of three legs, one for each phase, as shown in Fig.4.21. Each inverter leg is similar to the one used for describing the basic one-leg inverter in Section 4.2. Therefore, the output of each leg, for example \( v_{AN} \), (with respect to the negative dc bus), depends only on \( V_d \) and the switch status; the output voltage is independent of the output load current since one of the two switches in a leg is always on at any instant. Here, we again ignore the blanking time required in practical circuits by assuming the switches to be ideal. Therefore, the inverter output voltage is independent of the direction of the load current.

![Fig.4.21 Three-phase inverter.](image)

4.4.1 PWM IN THREE-PHASE VOLTAGE SOURCE INVERTERS

Similar to the single-phase inverters, the objective in pulse-width-modulated three-phase inverters is to shape and control the three-phase output voltages in magnitude and frequency with an essentially constant input voltage \( V_d \). To obtain balanced three-phase output voltages in a three-phase PWM inverter, the same triangular voltage waveform is compared with three sinusoidal control voltages that are 120° out of phase, as shown in Fig.4.22a (which is drawn for \( m_f = 15 \)).
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It should also be noted from Fig.4.22b that an identical amount of average dc component is present in the output voltages $v_{AN}$ and $v_{BN}$, which are measured with respect to the negative dc bus. These dc components are canceled out in the line-to-line voltages, for example in $v_{AB}$ shown in Fig.4.22b. This is similar to what happens in a single-phase full-bridge inverter utilizing a PWM switching.

In the three-phase inverters, only the harmonics in the line-to-line voltages are of concern. The harmonics in the output of any one of the legs, for example $v_{AB}$ in Fig.4.22b, are identical to the harmonics in $v_{A0}$ in Fig.4.5, where only the odd harmonics exist as sidebands, centered around $m_f$ and its multiples, provided $m_f$ is odd. Only considering the harmonic at $m_f$ (the same applies to its odd multiples), the phase difference between the $m_f$ harmonic in $v_{AN}$ and $v_{BN}$ is $(120 m_f)^\circ$. This phase difference will be equivalent to zero (a multiple of $360^\circ$) if $m_f$ is odd and a multiple of 3. As a consequence, the harmonic at $m_f$ is suppressed in the line-to-line voltage $v_{AB}$. The same argument applies in the suppression of harmonics at the odd multiples of $m_f$ if $m_f$ is chosen to be an odd multiple of 3 (where the reason for choosing $m_f$ to be an odd multiple of 3 is to keep $m_f$ odd and, hence, eliminate even harmonics). Thus, some of the dominant harmonics in the one-leg inverter can be eliminated from the line-to-line voltage of a three-phase inverter. PWM considerations are summarized as follows:

1. For low values of $m_f$, to eliminate the even harmonics, a synchronized PWM should be used and $m_f$ should be an odd integer. Moreover, $m_f$ should be a multiple of 3 to cancel out the most dominant harmonics in the line-to-line voltage.

2. For large values of $m_f$, the comments in Section 4.2.1.2 for a single-phase PWM apply.

3. During overmodulation ($m_a > 1.0$), regardless of the value of $m_f$, the conditions pertinent to a small $m_f$ should be observed.

4.4.1.1 Linear Modulation ($m_a \leq 1.0$)

In the linear region ($m_a \leq 1.0$), the fundamental-frequency component in the output voltage varies linearly with the amplitude modulation ratio $m_a$. From Figs.4.5b and 4.22b, the peak value of the fundamental-frequency component in one of the inverter legs is

$$\hat{V}_{AN} = m_a \frac{V_d}{2}$$

Therefore, the line-to-line rms voltage at the fundamental frequency, due to $120^\circ$ phase displacement between phase voltages, can be written as

$$V_{\text{LL}, \text{rms}} = \frac{\sqrt{3}}{2} \hat{V}_{AN} = \frac{\sqrt{3}}{2} m_a V_d = 0.612 m_a V_d \quad (m_a \leq 1.0)$$
4.4.1.2 Overmodulation \((m_d > 1.0)\)

In PWM overmodulation, the peak of the control voltages are allowed to exceed the peak of the triangular waveform. Unlike the linear region, in this mode of operation the fundamental-frequency voltage magnitude does not increase proportionally with \(m_a\). This is shown in Fig.4.23, where the rms value of the fundamental-frequency line-to-line voltage \(V_{LL1}\) is plotted as a function of \(m_d\). Similar to a single-phase PWM, for sufficiently large values of \(m_a\), the PWM degenerates into a square-wave inverter waveform. This results in the maximum value of \(V_{LL1}\) equal to 0.78 \(V_d\) as explained in the next section.

In the overmodulation region compared to the region with \(m_d \leq 1.0\), more sideband harmonics appear centered around the frequencies of harmonics \(mf\) and its multiples. However, the dominant harmonics may not have as large an amplitude as with \(m_d \leq 1.0\). Therefore, the power loss in the load due to the harmonic frequencies may not be as high in the overmodulation region as the presence of
additional sideband harmonics would suggest. Depending on the nature of the load and on the
switching frequency, the losses due to these harmonics in overmodulation may be even less than those
in the linear region of the PWM.

Table 2 Generalized Harmonics of $v_{LL}$ for a large and odd $m_f$ that is a multiple of 3.

<table>
<thead>
<tr>
<th>$h$</th>
<th>$m_a$</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>0.122</td>
<td>0.245</td>
<td>0.367</td>
<td>0.490</td>
<td>0.612</td>
</tr>
<tr>
<td>$m_f \pm 2$</td>
<td></td>
<td>0.010</td>
<td>0.037</td>
<td>0.080</td>
<td>0.135</td>
<td>0.195</td>
</tr>
<tr>
<td>$m_f \pm 4$</td>
<td></td>
<td>0.005</td>
<td>0.011</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$2m_f \pm 1$</td>
<td></td>
<td>0.116</td>
<td>0.200</td>
<td>0.227</td>
<td>0.192</td>
<td>0.111</td>
</tr>
<tr>
<td>$2m_f \pm 5$</td>
<td></td>
<td>0.008</td>
<td>0.020</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$3m_f \pm 2$</td>
<td></td>
<td>0.027</td>
<td>0.085</td>
<td>0.124</td>
<td>0.108</td>
<td>0.038</td>
</tr>
<tr>
<td>$3m_f \pm 4$</td>
<td></td>
<td>0.007</td>
<td>0.029</td>
<td>0.064</td>
<td>0.096</td>
<td></td>
</tr>
<tr>
<td>$4m_f \pm 1$</td>
<td></td>
<td>0.100</td>
<td>0.096</td>
<td>0.005</td>
<td>0.064</td>
<td>0.042</td>
</tr>
<tr>
<td>$4m_f \pm 5$</td>
<td></td>
<td>0.021</td>
<td>0.051</td>
<td>0.073</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$4m_f \pm 7$</td>
<td></td>
<td>0.010</td>
<td>0.030</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: $(V_{LL})_{av}/V_d$ are tabulated as a function of $m_a$, where $(V_{LL})_{av}$ are the rms
values of the harmonic voltages.

Fig. 4.23 Three-phase inverter $V_{LL}(rms)/V_d$ as a function of $m_a$.

4.4.2 SQUARE-WAVE OPERATION IN THREE-PHASE INVERTERS

If the input dc voltage $V_d$ is controllable, the inverter in Fig.4.24a can be operated in a square-wave
mode. Also for sufficiently large values of $m_a$, PWM degenerates into square-wave operation and the
voltage waveforms are shown in Fig.4.24b. Here, each switch is on for 180° (i.e., its duty ratio is 50%).
Therefore, at any instant of time, three switches are on.
In the square-wave mode of operation, the inverter itself cannot control the magnitude of the output ac voltages. Therefore, the dc input voltage must be controlled in order to control the output in magnitude. Here, the fundamental-frequency line-to-line \( \text{rms} \) voltage component in the output can be obtained from Eq. (13) for the basic one-leg inverter operating in a square-wave mode:

\[
V_{LL} \text{(rms)} = \frac{\sqrt{3}}{2} \frac{4V_d}{\pi}
\]

The line-to-line output voltage waveform does not depend on the load and contains harmonics \((6n \pm 1; n = 1, 2, \ldots)\), whose amplitudes decrease inversely proportional to their harmonic order, as shown in Fig. 4.24c:

\[
(V_{LL})_h = \frac{0.78}{h} V_d
\]

where \( h = n \pm 1 \) \((n = 1, 2, 3, \ldots)\)

It should be noted that it is not possible to control the output magnitude in a three-phase, square-wave inverter by means of voltage cancellation as described in Section 4.3.2.4.

### 4.4.3 SWITCH UTILIZATION IN THREE-PHASE INVERTERS

We will assume that \( V_{d,\text{max}} \) is the maximum input voltage that remains constant during PWM and is decreased below this level to control the output voltage magnitude in a square-wave mode. We will also assume that there is sufficient inductance associated with the load to yield a pure sinusoidal output current with an \( \text{rms} \) value of \( I_{o,\text{max}} \) (both in the PWM and the square-wave mode) at maximum loading. Therefore, each switch would have the following peak ratings:

\[
V_T = V_{d,\text{max}} \quad \text{(4.60)}
\]

and

\[
I_T = \sqrt{2} I_{o,\text{max}} \quad \text{(4.61)}
\]

If \( V_{LL1} \) is the \( \text{rms} \) value of the fundamental-frequency line-to-line voltage component, the three-phase output volt-amperes \( \text{(rms)} \) at the fundamental frequency at the rated output is

\[
(VA)_{3-\text{phase}} = \sqrt{3} V_{LL1} I_{o,\text{max}} \quad \text{(4.62)}
\]

Therefore, the total switch utilization ratio of all six switches combined is
Switch utilization ratio = \( \frac{(VA)_{3\text{-phase}}}{6V_L I_T} \)
\[ = \frac{\sqrt{3} V_{LL} I_{L,\max}}{6 V_{d,max} \sqrt{2} I_{a,\max}} \]
\[ = \frac{1}{2\sqrt{6} V_{d,max}} \]

In the PWM linear region \((m_a \leq 1.0)\) using Eq.(4.57) and noting that the maximum switch utilization occurs at \(V_d = V_{d,max}\)

Maximum switch utilization ratio (PWM)
\[ = \frac{1}{2\sqrt{6} \sqrt{2} m_a} \]
\[ = \frac{1}{2} m_a \quad (m_a \leq 1.0) \] (4.64)

In the square-wave mode, this ratio is \(1/2\pi \cong 0.16\) compared to a maximum of 0.125 for a PWM linear region with \(m_a = 1.0\).

In practice, the same derating in the switch utilization ratio applies as discussed in Section 4.3.4 for single-phase inverters.

Comparing Eqs.(4.54) and (4.64), we observe that the maximum switch utilization ratio is the same in a three-phase, three-leg inverter as in a single-phase inverter. In other words, using the switches with identical ratings, a three-phase inverter with 50% increase in the number of switches results in a 50% increase in the output volt-ampere, compared to a single-phase inverter.

### 4.4.4 RIPPLE IN THE INVERTER OUTPUT

Figure 4.25a shows a three-phase, three-leg, voltage source, switch-mode inverter in a block diagram form. It is assumed to be supplying a three-phase ac motor load. Each phase of the load is shown by means of its simplified equivalent circuit with respect to the load neutral n. The induced back \(e_A(t), e_B(t), \) and \(e_C(t)\) are assumed to be sinusoidal.

Fig.4.25 Three-phase inverter: (a) circuit diagram; (b) phasor diagram (fundamental frequency).

Under balanced operating conditions, it is possible to express the inverter phase output voltages \(v_{AN}, \) and so on (with respect to the load neutral n), in terms of the inverter output voltages with respect to the negative dc bus \(N:\)
\[ v_{kn} = v_{kN} - v_{nN} \quad (k = A, B, C) \] (4.65)

Each phase voltage can be written as
\[ v_{kn} = L \frac{di_k}{dt} + e_{kn} \quad (k = A, B, C) \] (4.66)

In a three-phase, three-wire load
\[ i_A + i_B + i_C = 0 \] (4.67a)
and
\[ \frac{d}{dt}(i_A + i_B + i_C) = 0 \] (4.67b)

Similarly, under balanced operating conditions, the three back-emfs are a balanced three-phase set of voltages, and therefore
\[ e_A + e_B + e_C = 0 \]  \hspace{1cm} (4.68)

From the foregoing equations, the following condition for the inverter voltages can be written:
\[ v_{An} + v_{Bn} + v_{Cn} = 0 \]  \hspace{1cm} (4.69)

Using Eqs. (4.65) through (4.69),
\[ v_{nN} = \frac{1}{3}(v_{AN} + v_{BN} + v_{CN}) \]  \hspace{1cm} (4.70)

Substituting \( v_{nN} \) from Eq.(4.70) into Eq.(4.65), we can write the phase-to-neutral voltage for phase A as
\[ v_{An} = \frac{2}{3}v_{AN} - \frac{1}{3}(v_{BN} + v_{CN}) \]  \hspace{1cm} (4.71)

Similar equations can be written for phase B and C voltages.

Similar to the discussion in Section 4.3.2.6 for the ripple in the single-phase inverter output, only the fundamental-frequency components of the phase voltage \( V_{An1} \) and the output current \( i_{A1} \) are responsible for the real power transformer since the back-emf \( e_A(t) \) is assumed to be sinusoidal and the load resistance is neglected. Therefore, in a phasor form as shown in Fig.4.25b
\[ V_{An1} = E_A + j\omega L I_{A1} \]  \hspace{1cm} (4.72)

By using the principle of superposition, all the ripple in \( v_{An} \) appears across the load inductance \( L \). Using Eq.(4.71), the waveform for the phase-to-load-neutral voltage \( V_{An} \) is shown in Figs.4.26a and 4.26b for square-wave and PWM operations, respectively. Both inverters have identical magnitudes of the fundamental-frequency voltage component \( V_{An1} \), which requires a higher \( V_d \) in the PWM operation. The voltage ripple \( v_{ripple}(=v_{An} - v_{An1}) \) is the ripple in the phase-to-neutral voltage.

Assuming identical loads in these two cases, the output current ripple is obtained by using Eq.(4.42) and plotted in Fig.4.26. This current ripple is independent of the power being transferred, that is, the current ripple would be the same so long as for a given load inductance \( L \), the ripple in the inverter output voltage remains constant in magnitude and frequency. This comparison indicates that for large values of \( m_f \), the current ripple in the PWM inverter will be significantly lower compared to a square-wave inverter.

![Fig.4.26 Phase-to-load-neutral variables of a three-phase inverter: (a) square wave: (b) PWM.](image)

4. 5 RECTIFIER MODE OF OPERATION
As we discussed in the introduction in Section 8-1, these switch-mode converters can make a smooth transition from the inverter mode to the rectifier mode. The rectifier mode of operation results, for example, during braking (slowing down) of induction motors supplied through a switch-mode converter. This mode of operation is briefly discussed in this section. The switch-mode rectifiers, used for interfacing power electronics equipment with the utility grid, operate on the same basic principle and are discussed in detail in Chapter 19.

The rectifier mode of operation is discussed only for the three-phase converters; the same principle applies to single-phase converters. Assuming a balanced steady-state operating condition, a three-phase converter is discussed on a per-phase basis.

As an example, consider the three-phase system shown in Fig. 8-25a, which is redrawn in Fig. 8-37a. Consider only the fundamental frequency (where the subscript 1 is omitted), neglecting the switching-frequency harmonics. In Fig. 8-37b, a motoring mode of operation is shown where the converter voltage $V_{an}$ applied to the motor leads $E_A$ by an angle $\delta$. The active (real) component $(I_A)_p$ of $I_A$ is in phase with $E_A$, and therefore the converter is operating in an inverter mode.

The phase angle (as well as the magnitude) of the ac voltage produced by the converter can be controlled. If the converter voltage $V_{an}$ is now made to lag $E_A$ by the same angle $\delta$ as before (keeping $V_{an}$ constant), the phasor diagram in Fig. 8-37c shows that the active component $(I_A)_p$ of $I_A$ is now 180° out of phase with $E_A$, resulting in a rectifier mode of operation where the power flows from the motor to the dc side of the converter.

In fact, $V_{an}$ can be controlled both in magnitude (within limits) and phase, thus allowing a control over the current magnitude and the power level, for example during the ac motor braking. Assuming that $E_A$ cannot change instantaneously, Fig. 8-37d shows the locus of the $V_{an}$ phasor, which would keep the magnitude of the current constant.

The waveforms of Fig. 8-22 can be used for explaining how to control $V_{an}$ in magnitude, as well as in phase, with a given (fixed) dc voltage $V_d$. It is obvious that by controlling the amplitude of the sinusoidal reference waveform $v_{control,a}$, $V_{an}$ can be varied. Similarly, by shifting the phase of $v_{control,a}$ with respect to $E_A$, the phase angle of $V_{an}$ can be varied. For a balanced operation, the control voltages for phases B and C are equal in magnitude, but ± 120° displaced with respect to the control voltage of phase A.

4.6 PROGRAMMABLE PWM CONVERTERS
This technique combines the square wave switching and PWM to control the fundamental output voltage as well as to eliminate the designated harmonics from the output voltage. This technique provides the facility to adjust the output voltage and simultaneous optimization of an objective function. The types of objective functions that technique can optimize are:

1- Selective harmonic elimination.
2- Minimum THD.
3- Reduced acoustic noise.
4- Minimum losses.
5- Minimum torque pulsations.

The main advantages of programmable PWM technique are:

1- High quality output voltage
2- About 50% reduction in switching frequency compared to conventional sine PWM.
3- Suitable for higher voltage and high power inverter systems, where switching frequency is a limitation.
4- Higher voltage gain due to over modulation.
5- Reduced size of dc link filter components.
6- Selective elimination of lower order harmonics guarantee avoidance of resonance with external line filtering networks.

The voltage $v_{Ao}$, of an inverter leg, normalized by $\frac{1}{2}V_d$ is plotted in Fig.4.34a, where six notches are introduced in the otherwise square-wave output, to control the magnitude of the fundamental voltage and to eliminate fifth and seventh harmonics. On a half-cycle basis, each notch provides one degree of freedom, that is, having three notches per half-cycle provides control of fundamental and elimination of two harmonics (in this case fifth and seventh).

Figure 4.38 shows that the output waveform has odd half-wave symmetry (sometimes it is referred to as odd quarter-wave symmetry). Therefore, only odd harmonics (coefficients of sine series) will be present. Since in a three-phase inverter (consisting of three such inverter legs), the third harmonic and its multiples are canceled out in the output, these harmonics need not be eliminated from the output of the inverter leg by means of waveform notching.

A careful examination shows that the switching frequency of a switch in Fig.4.38 is seven times the switching frequency associated with a square-wave operation.

In a square-wave operation, the fundamental-frequency voltage component is:

$$\frac{\left(\hat{v}_{Ao}\right)_{h}}{V_d/2} = \frac{4}{\pi} = 1.273$$  \hspace{1cm} (4.73)

Because of the notches to eliminate 5th and 7th harmonics, the maximum available fundamental amplitude is reduced. It can be shown that:

$$\frac{\left(\hat{v}_{Ao}\right)_{h,\text{max}}}{V_d/2} = 1.188$$  \hspace{1cm} (4.74)
It is clear that the waveform in Fig.4.38 is odd function. So,

\[ b_n = \frac{1}{n\pi} \sum_{s=1}^{m} J_s \cos n\alpha \]  \hspace{1cm} (4.75)

Where \( m \) is the number of jumps in the waveform. Jumps of the waveform shown in the figure is for only quarter of the waveform (because of similarity). The jumps are tabulated in the following table.

<table>
<thead>
<tr>
<th>( J_s )</th>
<th>( J_1 )</th>
<th>( J_2 )</th>
<th>( J_3 )</th>
<th>( J_4 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time</td>
<td>0</td>
<td>( \alpha_1 )</td>
<td>( \alpha_2 )</td>
<td>( \alpha_3 )</td>
</tr>
<tr>
<td>Value</td>
<td>2</td>
<td>-2</td>
<td>2</td>
<td>-2</td>
</tr>
</tbody>
</table>

Then, \( b_n = \frac{2}{n\pi} \left[ 2\cos n0 - 2\cos n\alpha_1 + 2\cos n\alpha_2 - 2\cos n\alpha_3 \right] \) \hspace{1cm} (4.76)

Where \( \alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2} \)

The above equation has three variables \( \alpha_1, \alpha_2, \text{and } \alpha_3 \) so we need three equation to obtain them. The First equation can be obtained by assigning a specific value to the amplitude of the fundamental component \( b_1 \). Another two equations can be obtained by equating \( b_5, \text{and } b_7 \) by zero to eliminate fifth and seventh harmonics. So, the following equations can be obtained.

\[ b_1 = \frac{4}{\pi} \left[ 1 - \cos \alpha_1 + \cos \alpha_2 - \cos \alpha_3 \right] \]  \hspace{1cm} (4.77)

\[ b_5 = \frac{4}{\pi} \left[ 1 - \cos 5\alpha_1 + \cos 5\alpha_2 - \cos 5\alpha_3 \right] = 0 \]  \hspace{1cm} (4.78)

\[ b_7 = \frac{4}{\pi} \left[ 1 - \cos 7\alpha_1 + \cos 7\alpha_2 - \cos 7\alpha_3 \right] = 0 \]  \hspace{1cm} (4.79)

The above equation can be rearranged to be in the following form:

\[
\begin{bmatrix}
\cos \alpha_1 & -\cos \alpha_2 & \cos \alpha_3 \\
\cos 5\alpha_1 & -\cos 5\alpha_2 & \cos 5\alpha_3 \\
\cos \alpha_1 & -\cos 7\alpha_2 & \cos 7\alpha_3
\end{bmatrix}
\begin{bmatrix}
\cos \alpha_1 \\
\cos 5\alpha_1 \\
\cos \alpha_1
\end{bmatrix}
= \begin{bmatrix}
1 - \frac{\pi b_1}{4} \\
1 \\
1
\end{bmatrix}
\]  \hspace{1cm} (4.80)

These equations are nonlinear having multiple solution depending the value of \( b_1 \). Computer programs help us in solving the above equations. The required values of \( \alpha_1, \alpha_2, \text{and } \alpha_3 \) are plotted in Fig.4.39 as a function of the normalized fundamental in the output voltage.
To allow control over the fundamental output and to eliminate the fifth-, seventh-, eleventh-, and the thirteenth-order harmonics, five notches per half cycle would be needed. In that case, each switch would have 11 times the switching frequency compared with a square-wave operation.

**Example** Eliminate fifth and seventh harmonics from square waveform with no control on the fundamental amplitude:

Solution: It is clear that we have only two conditions which are $b_5 = 0$ and $b_7 = 0$. So, we have only two notches per half cycle as shown in the following figure.

So we need only two variables $\alpha_1$ and $\alpha_2$ which can be obtained from the following equations:

$$b_n = \frac{4}{n\pi} \left[ 1 - \cos n\alpha_1 + \cos n\alpha_2 \right]$$  \hspace{1cm} (4.81)

$$b_5 = \frac{4}{\pi} \left[ 1 - \cos 5\alpha_1 + \cos 5\alpha_2 \right] = 0$$  \hspace{1cm} (4.82)

$$b_7 = \frac{4}{\pi} \left[ 1 - \cos 7\alpha_1 + \cos 7\alpha_2 \right] = 0$$  \hspace{1cm} (4.83)

$$\begin{bmatrix} \cos 5\alpha_1 & -\cos 5\alpha_2 \\ \cos 7\alpha_1 & -\cos 7\alpha_2 \end{bmatrix} \begin{bmatrix} 1 \\ 1 \end{bmatrix} = 0$$  \hspace{1cm} (4.84)

By solving the above equation we can get the value of $\alpha_1$ and $\alpha_2$ as following:

$\alpha_1 = 12.8111^\circ$ and $\alpha_2 = 24.8458^\circ$

The following table shows the absolute value of each harmonics after eliminating fifth and seventh harmonics.
### Chapter Three

#### Harmonic order

<table>
<thead>
<tr>
<th>Harmonic order</th>
<th>$b_n$ for square wave $b_n = \frac{4}{n\pi}$</th>
<th>$b_n$ after eliminating 5th and 7th</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.27324</td>
<td>1.1871</td>
</tr>
<tr>
<td>3</td>
<td>0.244413</td>
<td>0.20511</td>
</tr>
<tr>
<td>5</td>
<td>0.25468</td>
<td>0.0</td>
</tr>
<tr>
<td>7</td>
<td>0.18189</td>
<td>0.0</td>
</tr>
<tr>
<td>9</td>
<td>0.14147</td>
<td>0.0995</td>
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</tr>
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<td>0.07183</td>
</tr>
<tr>
<td>21</td>
<td>0.06063</td>
<td>0.00407</td>
</tr>
<tr>
<td>THD</td>
<td>22.669%</td>
<td>26.201%</td>
</tr>
</tbody>
</table>

#### 4.7 LOW COST PWM CONVERTER FOR UTILITY INTERFACE.

As discussed in regular three phase PWM inverter, the existing configuration uses six switches as shown in Fig.4.21. The low cost PWM inverter (Four switch inverter) uses four semiconductor switches. The reduction in number of switches reduces switching losses, system cost and enhances reliability of the system.

Fig.4.40 shows the proposed converter with four switches (Four Switch Topology, FST) By comparing Fig.4.40 and Fig.4.21, it is clear that, by using one additional capacitor one can replace two switches and the system will perform the same function. It is apparent that the cost and reliability are two major advantages of the proposed converter. The cost reduction can be accomplished by reducing the number of switches and the complexity of control system. The proposed converter current regulated with good power quality characterization.

![Four switch converter](image)

**Fig.4.40 Four switch converter.**

- **System Analysis**

For the proposed converter Fig.4.40, the switching requirements can be stated as follows.

Let the input three-phase generated voltages are:

\[ V_{ab} = \sqrt{3} * V_m \sin(\omega t + 30) \]

\[ V_{bc} = \sqrt{3} * V_m \sin(\omega t + 270) \]

\[ V_{ca} = \sqrt{3} * V_m \sin(\omega t + 150) \]

The line voltages at the generator terminals can be expressed as follows:

\[
\begin{bmatrix}
    V_{ab} \\
    V_{cb}
\end{bmatrix} =
\begin{bmatrix}
    S_1 & S_2 \\
    S_3 & S_4
\end{bmatrix} *
\begin{bmatrix}
    V_d \\
    -V_d
\end{bmatrix} / 2
\]

(4.86)
Where \( S_1, S_2, S_3 \) and \( S_4 \) are the switching functions of switches 1, 2, 3 and 4 respectively. \( V_d \) is the DC-link voltage.

But, \( S_2 = 1 - S_1 \) and \( S_4 = 1 - S_3 \) \hspace{1cm} (4.87)

\[
V_{ab} = (2S_1 - 1) \left( \frac{V_d}{2} \right) \text{ and}
\]

Then,

\[
V_{cb} = (2S_3 - 1) \left( \frac{V_d}{2} \right)
\]

Then from (4.85), (4.86), (4.87) and (4.88) we get the following equation:

\[
S_1 = 0.5 + \sqrt{3} \frac{V_m}{V_d} \sin(\omega t + 30^\circ)
\]

\[
S_2 = 0.5 - \sqrt{3} \frac{V_m}{V_d} \sin(\omega t + 30^\circ)
\]

\[
S_3 = 0.5 + \sqrt{3} \frac{V_m}{V_d} \sin(\omega t + 90^\circ)
\]

\[
S_4 = 0.5 - \sqrt{3} \frac{V_m}{V_d} \sin(\omega t + 90^\circ)
\]

Then, the shift angle for switching signal of leg ‘a’ is \( 30^\circ \) and for leg ‘c’ is \( 90^\circ \). Then,

\[
V_{ab} = m_a \frac{V_d}{2\sqrt{2}} \angle 30^\circ
\]

\[
V_{bc} = m_a \frac{V_d}{2\sqrt{2}} \angle 270^\circ
\]

\[
V_{ca} = m_a \frac{V_d}{2\sqrt{2}} \angle 150^\circ
\]

Then, \( V_{LL} = m_a \frac{V_d}{2\sqrt{2}} \)

(4.93)

From the above equations it is clear that the DC voltage must be at least twice the maximum of input line-to-line voltage to avoid the input current distortion.

The main disadvantage of four switch converter is it needs for higher dc voltage to give the same line-to-line voltage as the six switch inverter which is clear from comparing the following equations:

\[
V_{LL} = m_a \frac{V_d}{2\sqrt{2}} \quad \text{(four switch converter)}
\]

(4.94)

\[
V_{LL} = \sqrt{3} m_a \frac{V_d}{2\sqrt{2}} \quad \text{(six switch converter)}
\]

(4.95)
PROBLEMS

SINGLE PHASE

1- In a single-phase full-bridge PWM inverter, the input dc voltage varies in a range of 295-325 V. Because of the low distortion required in the output \(v_o\), \(m_a \leq 1.0\)

(a) What is the highest \(V_{o1}\), that can be obtained and stamped on its nameplate as its voltage rating?

(b) Its nameplate volt-ampere rating is specified as 2000 VA, that is, \(V_{o1,\text{max}}I_{o1,\text{max}} = 2000\text{VA}\), where \(i_o\) is assumed to be sinusoidal. Calculate the combined switch utilization ratio when the inverter is supplying its rated volt-amperes.

2- Consider the problem of ripple in the output current of a single-phase full-bridge inverter. Assume \(V_{o1} = 220\text{ V}\) at a frequency of 47 Hz and the type of load is as shown in Fig. 4.18a with \(L = 100\text{ mH}\). If the inverter is operating in a square-wave mode, calculate the peak value of the ripple current.

3- Repeat Problem 2 with the inverter operating in a sinusoidal PWM mode, with \(m_f = 21\) and \(m_a = 0.8\). Assume a bipolar voltage switching.

4- Repeat Problem 2 but assume that the output voltage is controlled by voltage cancellation and \(V_d\) has the same value as required in the PWM inverter of Problem 3.

5- Calculate and compare the peak values of the ripple currents in Problems 2 through 4.

THREE-PHASE

6- Consider the problem of ripple in the output current of a three-phase square-wave inverter. Assume \(V_{LL} = 220\text{ V}\) at a frequency of 52 Hz and the type of load is as shown in Fig. 4.25a with \(L = 100\text{ mH}\). Calculate the peak ripple current defined in Fig. 4.26a.

7- Repeat Problem 6 if the inverter of Problem 6 is operating in a synchronous PWM mode with \(m_f = 39\) and \(m_a = 0.8\). Calculate the peak ripple current defined in Fig. 4.26b.

8- In the three-phase, square-wave inverter of Fig. 4.24a, consider the load to be balanced and purely resistive with a load-neutral \(n\). Draw the steady-state \(v_{An}\), \(u_A\), \(i_{DA+}\), and \(i_d\) waveforms, where \(i_{DA+}\) is the current through \(DA+\).

9- Repeat Problem 8 by assuming that the load is purely inductive, where the load resistance, though finite, can be neglected.